# METHOD AND ARRANGEMENTS FOR FAST TRANSITION FROM A LOW POWER STATE TO A FULL POWER STATE IN A COMMUNICATION SYSTEM

## Background of the Invention

The present invention relates to a method to transit in a communication system from a low power state to a full power state as defined in the non-characteristic part of claim 1, an arrangement to be used to transit from the low power state to the full power state in a transmitter as defined in the non-characteristic part of claim 3, and an arrangement to transit from the low power state to the full power state in a receiver as defined in the non-characteristic part of claim 4.

Such a state transition method and arrangements to perform such a state transition are already known in the art, e.g. from *the temporary document WH-031 submitted on June 29, 1998 to ITU Study Group 15 which is an ADSL (Asymmetric Digital Subscriber Line) forum. This document with reference WH-031 is entitled 'Time Domain Rate Adaptation Based L1 State for G. Lite Modem Power Down Management' and originates from ITeX.* In this document, a mechanism for transition between a so called L1 state, a low power/low bit rate state, to a so called L0 state, a full power/full bit rate state, of an ADSL (Asymmetric Digital Subscriber Line) system is described. As is indicated in paragraph 2 of the cited document, transition between the low power and the full power state is initiated by transfer of a predetermined recognisable state transition indication, called EOC message. Thereafter, the new state is entered at the beginning of the next super-frame. The transition time to switch from the low power state to the full power state is not minimised in the known solution because the actual transition from the low power state to the full power state is delayed until the beginning of the next super-frame. In particular in systems such as the known one, wherein data are transferred at a low bit rate during the low power state, the transition time can become significantly large, i.e. several multiples of the time interval required to transfer a super-frame at full power. In communication systems with

buffers temporarily storing data, large state transition times imply increased probability for buffer overflow, congestion and even loss of data. If for instance ATM (Asynchronous Transfer Mode) cells have to be transferred over an ADSL (Asymmetric Digital Subscriber Line) network segment, risk of ATM buffer overflow increases if the wake-up time, i.e. the transition time from the low power state to the full power state of the ADSL network segment is large.

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## Summary of the Invention

An object of the present invention is to provide a method and arrangements for transition from the low power state to the full power state similar to the known one, but wherein the wake-up time to go from the low power state to the full power state is minimised.

According to the invention, this object is achieved by the method to transit in a communication system from a low power state to a full power state as defined in claim 1, an arrangement to be used to transit from the low power state to the full power state in a transmitter as defined in claim 3, and an arrangement to transit from the low power state to the full power state in a receiver as defined in claim 4.

Indeed, since the time to transfer the remainder of a data packet in the low power state may succeed several times the time required to transfer a complete data packet in the full power state, the transition time from the low power state to the full power state may be reduced if the low power transmission is abruptly interrupted, and if the remainder of the data packet currently transferred, is not transmitted at low power. Depending on the remainder of the data packet that still had to be transferred at low power, which is a statistical parameter, and on the difference in transfer time between a full power data packet and a low power data packet, the transition time from the low power state to the full power state will be increased or not. In communication systems wherein the bit rate in the full power state is several multiples of the bit rate in the low power state, the average wake-up time from the low power state to the full power state will be significantly reduced. The incompletely transferred low power data packet for evident reasons can not be used at the receiver's side and

consequently it is required to re-send at full power the whole data packet whose transfer has been interrupted.

It is to be noticed that the term 'comprising', used in the claims, should not be interpreted as being limitative to the means listed thereafter. Thus, the scope of the expression 'a device comprising means A and B' should not be limited to devices consisting only of components A and B. It means that with respect to the present invention, the only relevant components of the device are A and B.

sub B4 An additional feature of the transition method from low power to full power state according to the present invention is defined in claim 2.

Thus, similar to what happens in the known transition method, the transition from the low power state to the full power state may be announced by sending a predetermined state transition indication from the transmitter to the receiver. The receiver can detect this state transition indication for example by correlation techniques. Alternatively, provided that the receiver is able to discriminate a data packet transmitted at full power from a data packet transmitted at low power, the transition from the low power state to the full power state can be initiated by transmitting a data packet at full power without first transmitting a predetermined state transition indication. The latter alternative requires a more complex receiver equipped with a power measurement device, but enables to even more reduce the transition time from the low power state to the full power state.

Brief Description of the Drawings

The above mentioned and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompanying drawings wherein:

Fig. 1 is a functional block scheme of a communication system with a transmitter TX and receiver RX including state transition arrangements STA and STA' according to the present invention; and

Fig. 2 is a data symbol flow diagram illustrating transition from the low power state LPS to the full power state FPS according to the known method in Fig. 2A, and illustrating transition from the low power state LPS to the full power state FPS according to a preferred implementation of the present invention in Fig. 2B.

## Detailed Description of the Invention

The communication system drawn in Fig. 1 contains an ADSL (Asymmetric Digital Subscriber Line) transmitter TX, a twisted pair telephone line CM, and an ADSL receiver RX. The ADSL transmitter includes a activity detector AD and a state transition arrangement STA comprising a DMT (Discrete Multi Tone) transmitter TXM, an interrupting device IR and a state transition indication generator STIG. The ADSL receiver RX includes a state transition indication detector STID and a state transition arrangement STA' comprising a DMT (Discrete Multi Tone) receiver RXM, a control unit CTRL, an interrupted symbol detector DET, and an interrupted symbol deletion device DEL.

In the ADSL transmitter TX, the DMT transmitter TXM is coupled between an input terminal of the ADSL transmitter TX adapted to receive ATM (Asynchronous Transfer Mode) cells and an output terminal of the ADSL transmitter TX adapted to source DMT (Discrete Multi Tone) symbols. The activity detector AD is coupled to the input terminal of the ADSL transmitter TX and is provided with an output terminal coupled respectively to inputs of the interruption device IR and the state transition indication generator STIG. An output of the interruption device IR is connected to a control input of the DMT transmitter TXM whereas an output of the state transition generator STIG is connected to an input terminal of the DMT transmitter TXM.

In the ADSL receiver RX, the DMT receiver RXM is coupled between an input terminal of the ADSL receiver RX adapted to receive DMT (Discrete Multi Tone) symbols and an output terminal of the ADSL receiver RX adapted to source ATM (Asynchronous Transfer Mode) cells. The state transition indication detector STID is coupled to the input terminal of the ADSL receiver RX and is provided with an output terminal coupled respectively to inputs of the control unit CTRL and the interrupted symbol detector DET. An output of the latter interrupted symbol

detector DET is connected to an input terminal of the interrupted symbol deletion device DEL, whereas an output of the control unit is connected to a control input of the DMT receiver RXM. The twisted pair telephone line CM is coupled between the output terminal of the ADSL transmitter TX and the input terminal of the ADSL receiver RX.

Although an ADSL (Asymmetric Digital Subscriber Line) system bi-directionally transfers digital data in overlay of telephone signals between a central office and remote terminal, the communication system in Fig. 1 shows transfer of data in only one direction, i.e. from the central office to the remote terminal or from the remote terminal to the central office. This uni-directional communication system nevertheless is supposed to operate in accordance with the ADSL principles: incoming data like for instance ATM (Asynchronous Transfer Mode) cells or IP 5Internet Protocol) packets are encapsulated in DMT (Discrete Multi Tone) symbols by the DMT transmitter TXM, whose working is based on an inverse Fourier transformer, and transmitted over the telephone line CM. At the receiver's side, the DMT symbols are de-capsulated by the DMT receiver RXM, whose working is based on a Fourier transformer, and the so generated ATM cells or IP packets are sourced. In case the ATM cells or IP packets at the entrance of the ADSL transmitter TX are not idle, the ADSL transmitter TX and ADSL receiver RX operate in a full power mode wherein the DMT symbols are transferred at high bit rate over the telephone line CM. In case the ATM cells or IP packets at the entrance of the ADSL receiver TX are idle, the ADSL transmitter TX and ADSL receiver RX operate in a low power mode wherein the DMT symbols are transferred at low bit rate over the telephone line CM. In the low power mode, power consumption of the ADSL transmitter TX and ADSL receiver RX is significantly reduced compared to the full power mode.

When the transmitter is in the low power mode, the activity detector AD monitors the entrance of the ADSL transmitter TX for non-idle ATM cells. As soon as the activity detector detects non-idle ATM cells at the input, the state transition indication generator STIG and the interruption device IR are triggered via control

signals. The state transition indication generator STIG generates a message with a predetermined contents and applies this message to the DMT transmitter TXM. The interruption means controls the DMT transmitter TXM to interrupt transmitting the low power DMT symbol DMT1 it is transmitting at that moment. As soon as transfer of the currently transferred low power DMT symbol DMT1 has been interrupted, the DMT transmitter TXM sends the predetermined message, the so called state transition indication STI, generated by the state transition indication generator STIG over the telephone line CM. Afterwards, the DMT transmitter TXM sends a copy C_DMT2 of the DMT symbol DMT1 whose transfer has been interrupted upon instruction of the interruption device IR. This copy C_DMT1 is no longer transmitted at low power but is transmitted at full power/full bit rate. The ADSL transmitter TXM has entered the full power state and will remain transmitting subsequent DMT symbols DMT2 at full power/full bit rate until idle ATM cells are applied to its input. The transition from the low power state LPS to the full power state FPS upon detection of non-idle ATM cells (Activity Detection) at the transmitter's entrance, whereby low power transfer of a DMT symbol DMT1 is interrupted and followed by full power transmission of the state transition indication STI, the copy C_DMT1 of the interrupted DMT symbol DMT1 and subsequent non-idle DMT symbols DMT2 is illustrated by Fig. 2B.

In the ADSL receiver RX, the state transition indication detector STID monitors the entrance of the ADSL receiver RX when this ADSL receiver RX operates in the low power state. The state transition indication detector STID for example uses correlation techniques to recognise the predetermined state transition indication STI send out by the ADSL transmitter TX to indicate transition from the low power state LPS to the full power state FPS. As soon as the state transition indication detector DET recognises the state transition indication STI, it activates the control unit CTRL and the interrupted symbol detector DET via control signals. The interrupted symbol detector DET detects the incompletely transmitted DMT symbol DMT1 that will be deleted by the interrupted symbol deletion device DEL. the control unit CTRL instructs the DMT receiver RXM to enter

the full power state FPS wherein it is able to receive subsequent DMT symbols C_DMT1, DMT2 at full power/full bit rate.

It is remarked that the functionality of the interrupted symbol detector DET and the interrupted symbol deletion device DEL may in an alternative embodiment of the present invention be integrated with the DMT receiver RXM into a single device. Indeed, the detection and deletion of incompletely transferred DMT symbols may be realised in hardware or in software and evidently can be integrated in the DMT receiver RXM.

It is also noticed that in an alternative version of the current invention, the average transition time from the low power state LPS to the full power state FPS is even more reduced by interrupting transmission of the currently transferred low power DMT symbol DMT1 only if that part of the DMT symbol DMT1 that has already been transmitted has not yet exceeded a certain threshold. Thus, the threshold can be selected so that transmission of the currently transferred DMT symbol DMT1 will be interrupted only if the copy C_DMT1 of this DMT symbol DMT1 can be transferred faster at full power than the remainder of the DMT symbol DMT1 can be transferred at low power. This implementation of the present invention minimises the average wake-up time to go from the low power state LPS to the full power state FPS at the cost of some additional complexity in the ADSL transmitter TX to determine the portion of the DMT symbol DMT1 that already has been transferred and to compare this portion with a certain threshold.

Furthermore, it is remarked that the activity detector AD may be able to check whether incoming data is idle or not, similar to the above described activity detector AD, but alternatively may just be able to interpret a control signal received from equipment interfacing the ADSL transmitter TX. This control signal may indicate that the data applied to the input terminal of the ADSL transmitter TX are idle or that no data at all are applied to the input terminal of the ADSL transmitter TX so that the low power state may be entered.

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Although it has been mentioned in the introductory part of this patent application, it is emphasised here that to implement the basic idea of the present invention, i.e. interrupting low power transmission of the currently transferred DMT symbol and full power transmission of a copy C_DMT1 of the interrupted DMT symbol DMT1, it is not required to generate, transfer and detect a state transition indication STI. Such a state transition indication STI helps the receiver RX to detect the moment whereon it has to transit from the low power state LPS to the full power state FPS, but must for example not be sent in a system wherein the receiver RX is able to detect the difference between a low power DMT symbol DMT1 and a full power DMT symbol DMT2 and is able to autonomously switch from the low power mode LPS to the full power mode FPS thereupon.

Also a remark is that various ways to implement the interrupted symbol deletion device DEL can be thought of. The bits of an interrupted DMT symbol can for example be taken from the line by a kind of switch. Alternatively, the bits can be made idle or zero.

Yet another remark is that the applicability of the invention is not reduced to telecommunication systems with a particular physical transmission medium or wherein any particular physical layer transmission protocol is used. The invention in other words can be applied in any packet or symbol based transmission system, irrespective of the fact whether the packets or symbols are sent over twisted pair cables, coaxial cables, optical fibres, radio links, satellite links, or the like, and irrespective of the physical layer protocol (e.g. ADSL - Asymmetric Digital Subscriber Line) that is used to represent the bits on the transmission link.

Furthermore, it is remarked that an embodiment of the present invention is described above in terms of functional blocks. From the functional description of these blocks it will be obvious for a person skilled in the art of designing electronic devices how embodiments of these blocks can be manufactured with well-known electronic components. A detailed architecture of the contents of the functional blocks hence is not given.

While the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation on the scope of the invention.